

**REMARKS**

Applicants have cancelled claims 2, 11, 22, and 30 and amended claims 1, 3, 10, 12, 21, 23, 29, and 31. In view of the following amendments and remarks, Applicants hereby request further examination and reconsideration of the application, and allowance of claims 1, 3-10, 12-21, 23-29, and 31.

The Office has rejected claims 1-6, 10-15, 19-26 and 29-31 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,635,705 to Saunders and claims 7-9, 16-18, 27 and 28 under 35 U.S.C. 103(a) as being unpatentable over Saunders. The Office asserts that Saunders discloses a signal processing system comprising a bus systems for transferring information data (video) signals from a plurality of signal streams to an output including a plurality of signal buses (20, 28, 32) in parallel and a control device (38, 34, 40, 48) for multiplexing the signals from two or more signal streams onto two or more signal buses and allowing the signals to substantially charge each of the signal buses before demultiplexing the signals to the output. The Office asserts that Saunders fails to specify the type of encoder being used but asserts that selecting a particular decoder for decoding signal in a signal processing system would have been a mere of routine skill in the art. The Office also asserts that the selection of further components for the control device recited in claims 9, 18 would have been obvious for similar reasons set forth above.

Saunders does not disclose or suggest, "the control system provides binning by coupling the signals from two or more adjacent signals buses in the plurality of signal buses to the output at substantially the same time to average the signals on these signal buses together" as recited in claims 1, 10, and 21, or "binning by coupling the signals from two or more adjacent signals buses in the plurality of signal buses to the output at substantially the same time to average the signals on these signal buses together" as recited in claim 29. The Office's attention is respectfully directed to FIG. 1 and col. 3, lines 22-24 in Saunders which states that, "the comparator outputs a digital signal on line 46 to a logic controller 48 which causes the logic controller and multiplexer to connect that input channel to one of the output processor channels." Accordingly, Saunders simply discloses passing a single input signal to one output channel. Nowhere does Saunders teach or suggest binning of two or more of these signals, let alone binning of two or more of these signals in a bus system where the two or more signals have been allowed to substantially charge on two or more buses before being output for binning. As discussed on page 17, lines 5-6 in the above-identified patent

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application, the present invention allows for a higher speed of operation by transferring input signal to different signal buses and allowing the signal buses to substantially charge before being selected to be output and also gives a new method of binning pixels at this higher rate of operation. Accordingly, in view of the foregoing amendments and remarks, the Office is respectfully requested to reconsider and withdraw the rejection of claims 1, 10, 21, and 29. Since claims 4-9 depend from and contain the limitations of claim 1, claims 14-20 depend from and contain the limitations of claim 10, and claims 24-28 depend from and contain the limitations of claim 21, they are distinguishable over the cited reference and are patentable in the same manner as claims 1, 10, and 21.

Saunders does not disclose or suggest, "the control system provides interpolation by coupling the two or more of the signals from the plurality of signal buses to the output separately and between coupling the two or more of the signals from the plurality of signal buses to the output separately, coupling each of the signals from adjacent pairs of the plurality of signal streams to the output at substantially the same time to obtain an interpolated signal" as recited in claims 3, 12, and 23, or "interpolating by coupling the two or more of the signals from the plurality of signal buses to the output separately and between coupling the two or more of the signals from the plurality of signal buses to the output separately, coupling each of the signals from adjacent pairs of the plurality of signal streams to the output at substantially the same time to obtain an interpolated signal" as recited in claim 31. Again the Office's attention is respectfully directed to FIG. 1 and col. 3, lines 22-24 in Saunders which states that, "the comparator outputs a digital signal on line 46 to a logic controller 48 which causes the logic controller and multiplexer to connect that input channel to one of the output processor channels." Accordingly, Saunders simply discloses passing a single input signal to one output channel. Nowhere does Saunders teach or suggest interpolating to find interpolation signals between two or more of the input signals, let alone interpolating to find interpolation signals in a bus system where the two or more signals have been allowed to substantially charge on two or more buses before being output for interpolation. As discussed on page 17, lines 5-6 in the above-identified patent application, the present invention allows for a higher speed of operation by transferring input signal to different signal buses and allowing the signal buses to substantially charge before being selected to be output and also gives a new method of binning pixels at this higher rate of operation. In view of the foregoing amendments and remarks, the Office is respectfully requested to reconsider and withdraw the rejection of claims 3, 12, 23, and 31.

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In view of the above amendments and the following remarks, reconsideration of the outstanding office action is respectfully requested. Pursuant to 37 CFR § 1.121, attached as Appendix A is a Version With Markings to Show Changes Made.

In view of all of the foregoing, applicants submit that this case is in condition for allowance and such allowance is earnestly solicited.

Respectfully submitted,

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